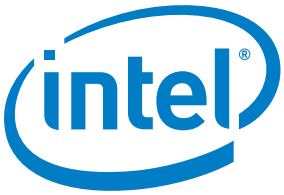

# Schematic Checking Tool Violations Report User Guide

## User Guide

***June 2016***

Document Number: 052785-1.1

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## Figures

# Revision History

| Document Number | Revision Number | Description | Revision Date |
|---|---|---|---|
| 052785 | 1.0 | • Initial release | May 2015 |
| 052785 | 1.1 | • Updated contact information to Customer Solutions Team | June 2016 |

§

# 1 Introduction

Schematic Checking Tool Violations and Decoupling Report Interpretation for customers receiving an Initial Report from the Customer Solutions Team Schematic Review Service Bureau using the Intel Schematic Checking Tool.

This document describes first how to interpret the Violations Report, followed by how to interpret the Decoupling Report.

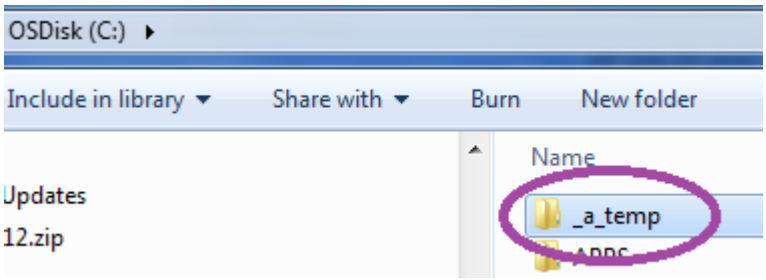
# 2 Violations Report Interpretation

The Schematic Checking Tool is an automated tool that compares point to point circuit topologies found in Rule Modules to those found in a design, expressing any differences as Violations. Customer Reference Boards are used as a starting point for Customer Solutions Team engineers to develop rule modules, and then the rules are edited using Platform Design Guides and External Data Specification documents to exclude test hooks or other circuitry that the customer design will most likely not include. Each pin of the device is given rules and tested one at a time as the Root Pin of a Rule.

The Initial Report you receive from CST.Services@intel.com is typically a single compressed file in WinZip format. The best way to review the report is to create a new directory and use WinZip to extract the files:

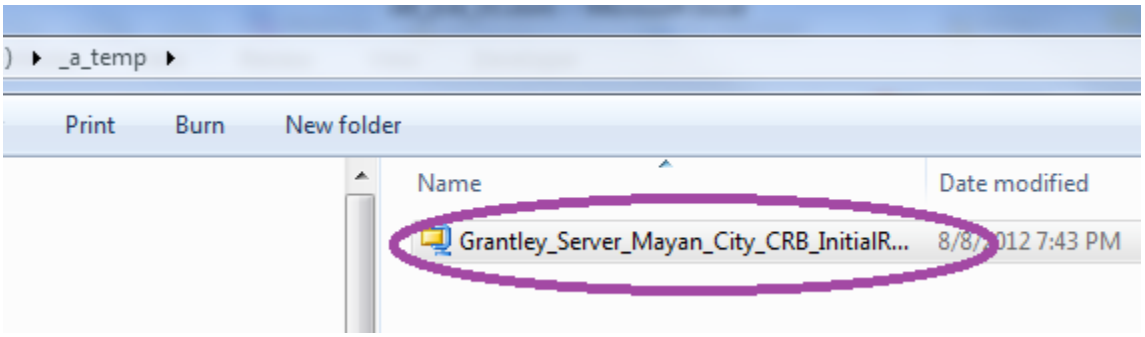
Make a temporary folder.

**Figure 1. Temporary File**



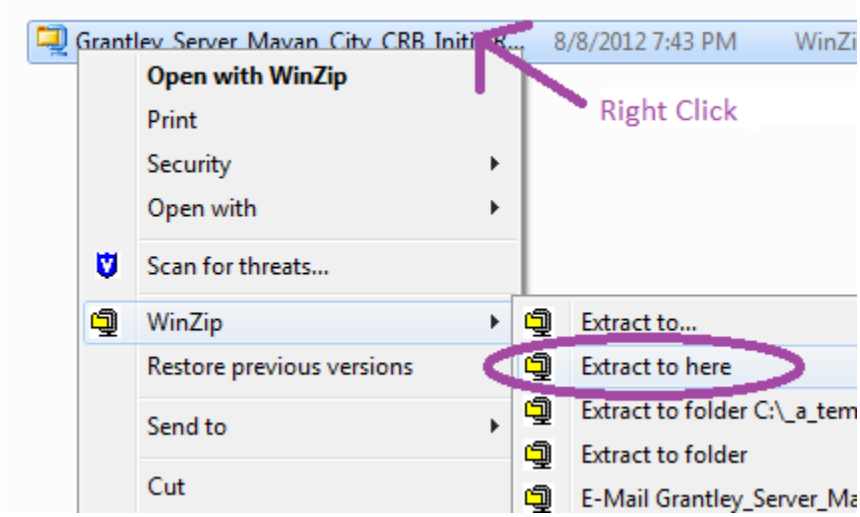

Paste the Initial Report Zip file in the temporary folder.

**Figure 2. Initial Report**



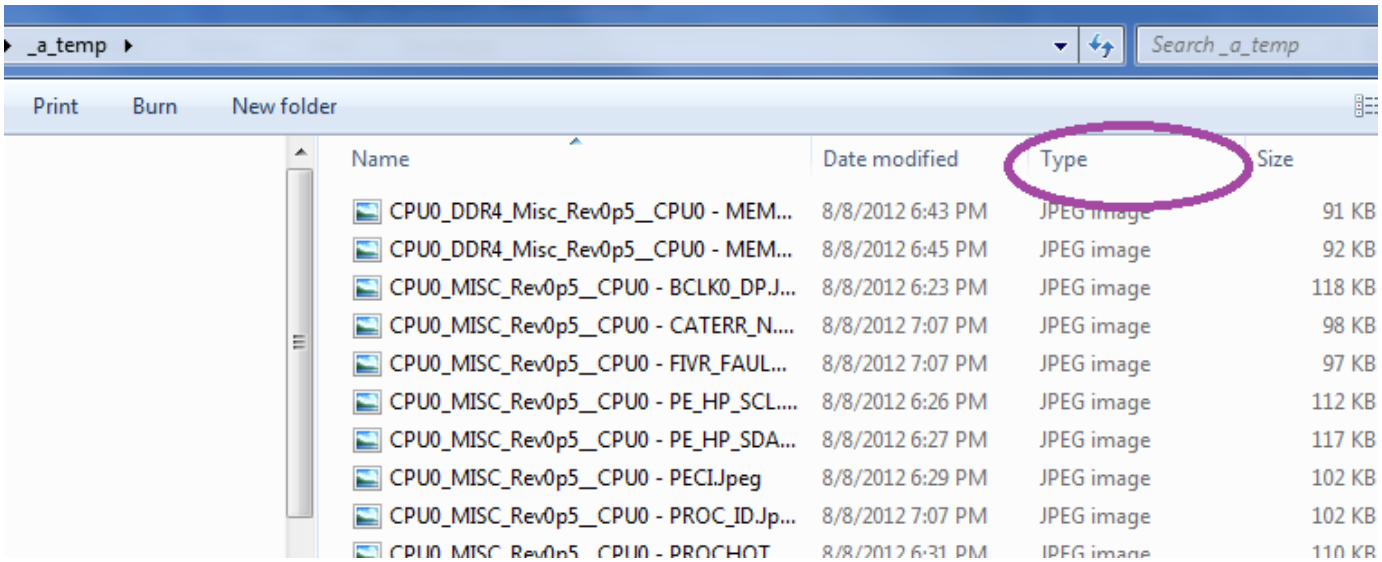
Right Click and select Extract to Here (WinZip needs to be installed on the system)

**Figure 3. Extract File**



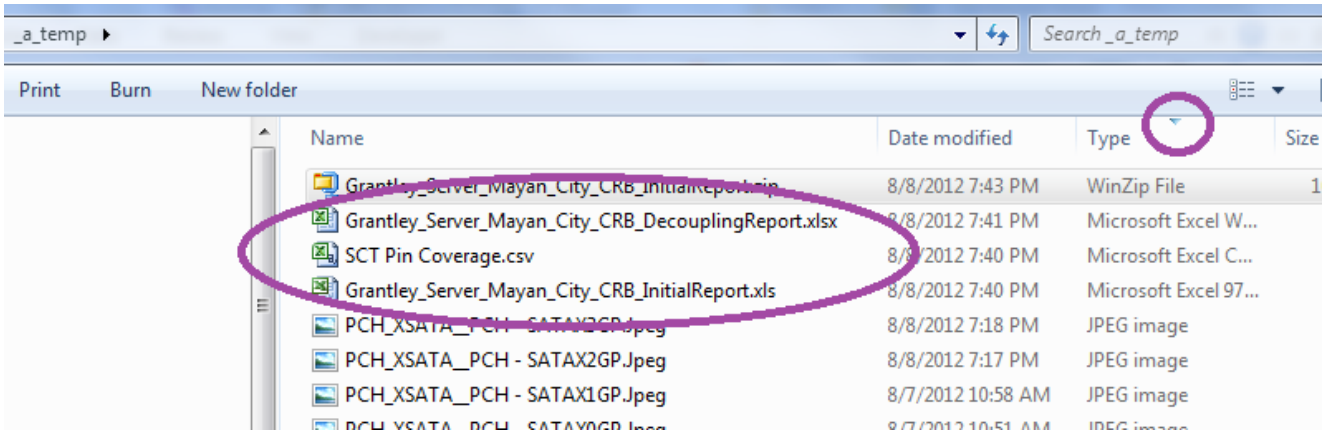

Click on Type to Sort by file Type, descending.

**Figure 4. Sort by Type**



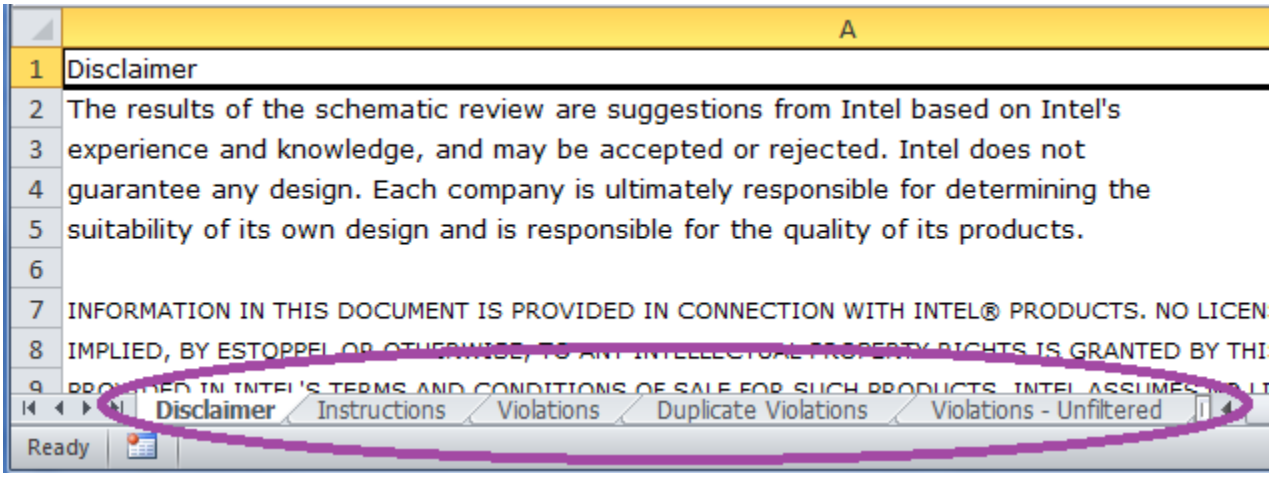
This makes the reports easy to find.

**Figure 5. Report Files**



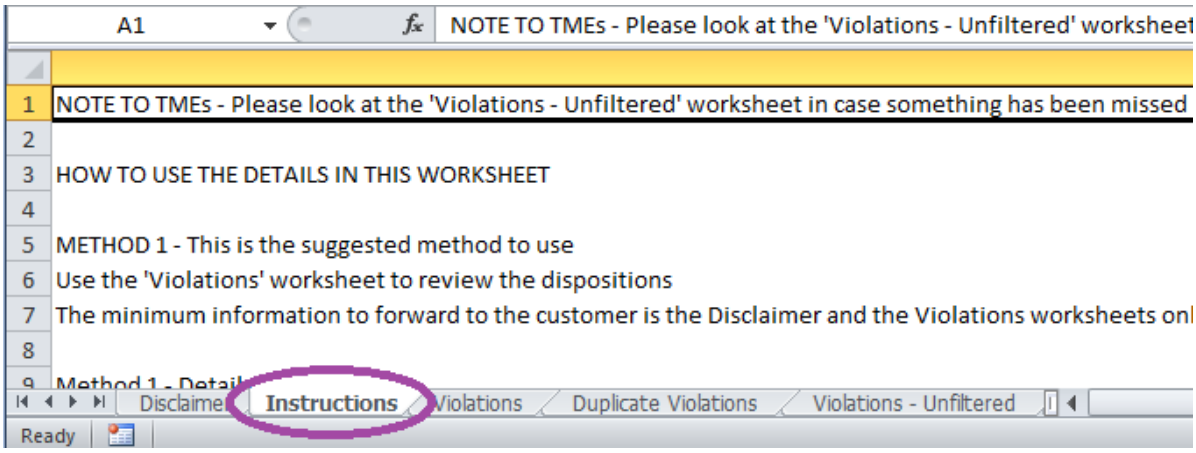

Open Initial Report.xlsx, see tabs shown.

**Figure 6. Report Tabs**



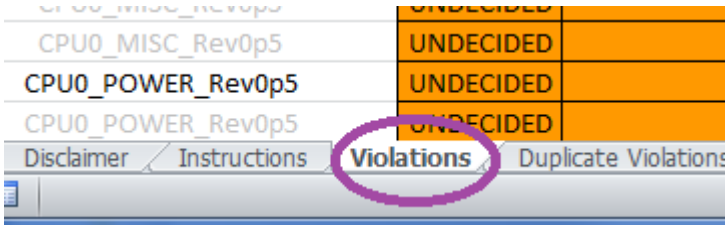
Please read instructions sheet for first time reviews.

**Figure 7. Instructions Tab**



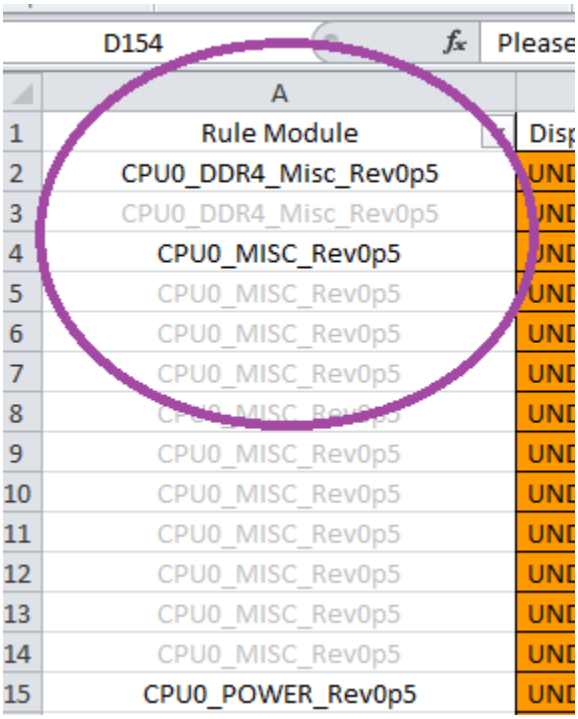

Violations tab has most of the information.

**Figure 8. Violations Tab**



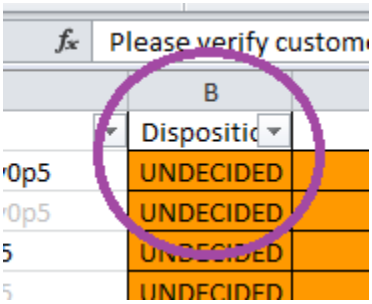
Column A shows the name of the Rule / Violation module for reference.

**Figure 9. Rule Module Applied Column**




Column B shows Disposition given by the review engineer. Need To Fix shows as red, Undecided shows as Orange, Info Only as Yellow.

**Figure 10. Disposition Column**




Need To Fix is given to violations of the PDG requirement that appear to be a Board Spin, that is, the signal will not function properly without changing more than just component values in the material list. It would require changing the layout of the board if not implemented before taping out.

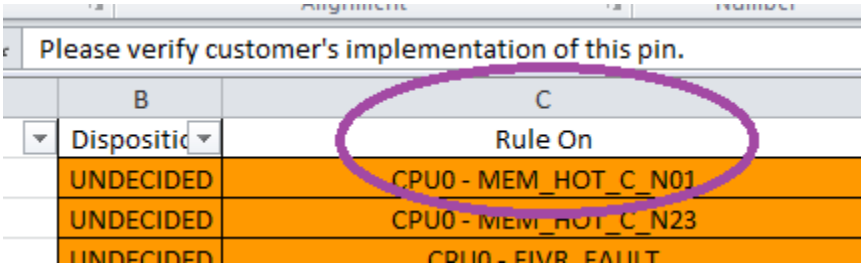
Undecided is given to violations that may be user definable, or vary from the Intel Platform Design Guidelines requirements such that the user may need to verify their intended functionality. This is also given to any violation where the reviewer is not sure, because we would rather call out a false violation than to not include something that may prove to be important.

Info Only is given to violations that are component values that vary from the PDG requirements. It is not unusual for Pull Ups and Pull downs to use incorrect values that may work perfectly well in the circuit, so these are shown as the lowest priority.

Waived violations do not appear in the Violations tab, these are only included in the Violations – Unfiltered tab. We recommend you check here to ensure we did not waive something that may be important.

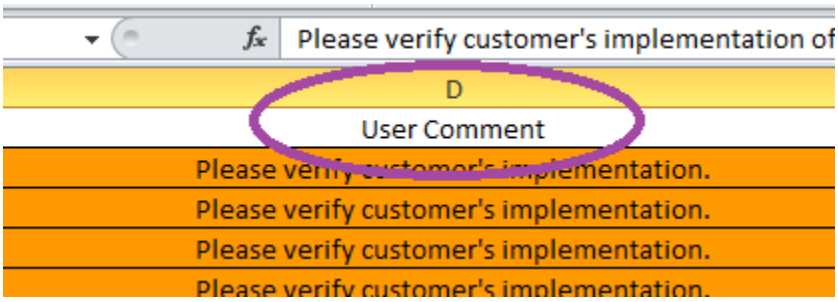
Column C is entitled Rule On, this is the Pin Name of the Root Device to which the rule is being applied. In this example, CPU0 pin MEM_HOT_C_N01 is a violation disposed as Undecided.

**Figure 11. Pin or Root Device**



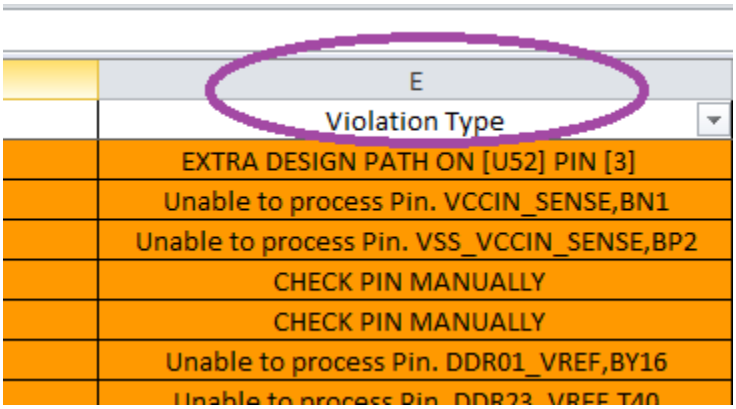

Column D is entitled User Comment, these are comments from the reviewer, or the default comments generated by the report generation automation, as in this case being "Please verify customer's implementation" for a violation disposed as Undecided.

**Figure 12. User Comments Column**



Column E is entitled Violation Type. These are comments generated by the Schematic Checking Tool. If the reviewer does not type in user comments manually, there are default comments added by the report generation automation. Here are the possible violations and notes about each:

**Figure 13. Violation Type Column**




Violation: "WRONG PIN"

Default automated user comment: "Pin number does not match expected pin number."

Note: This indicates that the pin number of the end point device pin in a path does not match the pin number in the rule. This is frequently a false violation that gets a "WAIVE" disposition when the reviewer recognizes that it is an equivalent pin type on a known device, such as one of several equivalent 100MHz clock buffer output pins.

Violation: "WRONG VALUE"

Default automated user comment: "INFO ONLY"

Note: This is for resistor, capacitor, and inductor values in Ohms, Micro-Farads, and Micro-Henrys.

Violation: "WRONG TOLERANCE"

Default automated user comment: "Please verify customer's implementation."

Note: This is for resistor, capacitor, and inductor value tolerances in Percent (%).

Violation: "EXTRA COMPONENT..."

Default automated user comment: "Please verify customer's implementation."

Note: This indicates that there were additional components not required by the rule, manual review is needed to determine if they are detrimental to the design.

Violation: "DUPLICATE PULLUP..." No Severity value, no Screen Shot for Generic

Default automated user comment: "Parallel components."

Note: This indicates that two or more components were connected in parallel as pull ups or pull downs on the same signal line.

Violation: "EXTRA DESIGN PATH..."

Default automated user comment: "Additional circuitry, please verify customer's implementation."

Note: This indicates that there is an extra end point device pin not required in the rule. Series components leading to extra design paths are not checked.

Violation: "CHECK PIN MANUALLY"

Default automated user comment: "Please verify customer's implementation."

Note: This is a rule type which unconditionally forces a violation, typically for circuits such as GPIO that have customized functionality not covered by PDG rules.

Violation: "NO CONNECT Violation"

Default automated user comment: "Unexpected connection."

Note: This indicates that a pin such as a Reserved pin which the PDG requires to be floating has been found to have circuitry attached.

Violation: "WRONG POPULATED PROP"

Default automated user comment: "Component load option not correct."

Note: This indicates that the Stuff or No Stuff property is either unreadable, or is the incorrect value.

Violation: "NO MATCHING PATH ENDING..."

Default automated user comment: "Required connection not present."

Note: This indicates that a required end point device pin in the rule was not found, meaning that either the circuit had fewer end points than required, or there is an issue with the part number identification of the end point device not matching the part number identification of the end point device in the rule.

Violation: "MISSING COMPONENT IN DESIGN..."

Default automated user comment: "Required component not present."

Note: This indicates that a required end point making a path that matches the rule is missing a required series component.

Violation: "Unable to process Pin..."

Default automated user comment: "Untested topology, please check manually."

Note: This indicates that the software encountered parallel paths and got caught in an endless loop, meaning that the topology algorithm was aborted with an error and there was no Design View produced for this circuit. The circuit must be reviewed manually using the PDF schematic.

Violation: "VOLTAGE TYPE CHECK ON..."

Default automated user comment: "Please verify proper Standby or Core voltage supply."

Note: This indicates that either the voltage is not the correct type, as in Standby or Core voltage type.

Violation: "DEVICE TYPES MISMATCH..."

Default automated user comment: "Please verify component equivalence to required component."

Note: This indicates that a path ending in a device pin matches a rule, except for the device type identification of the device.

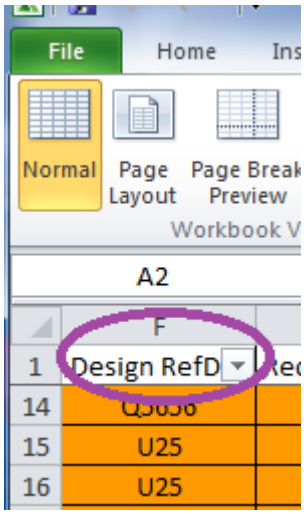
Violation: "VOLTAGE VALUE CHECK ON..."

Default automated user comment: "Please verify proper voltage being applied."

Note: This indicates that the numeric voltage value found on the voltage net does not match the rule.

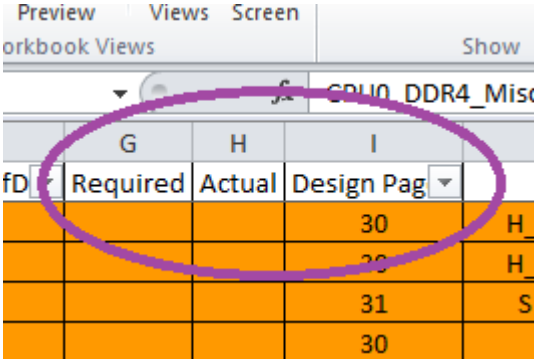
Column F is entitled "Design RefDes" to show the Reference Designator of the root device pin in the rule.

**Figure 14. Reference Designators Column**



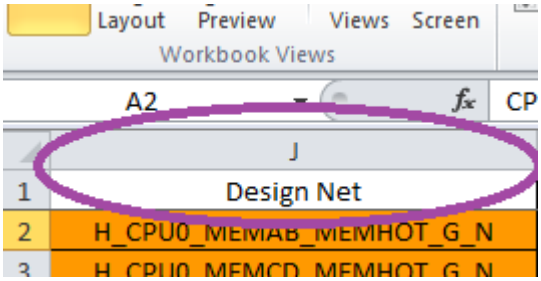

Columns G, H and I are entitled "Required", "Actual", and "Design Page", respectively. Required and Actual are used only for Value and Tolerance violations to show what was required and what was found in the design. Actual value of Zero or Null may indicate that the properties in the design were not readable by the Schematic Checking Tool. Design Page indicates the PDF schematic page number upon which the root device pin in the rule may be found.

**Figure 15. Required, Actual, and Design Page Columns**



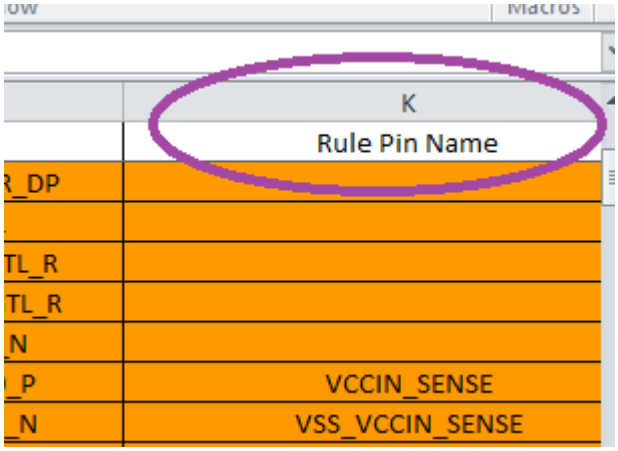
Column J is entitled "Design Net" to show the net name of the node attached to the root device pin in the rule.

**Figure 16. Design Net Column**




Column K is entitled "Rule Pin Name" to show the pin name if it would otherwise not appear in the Rule View of the Graphics Violation Viewer, as is the case with Check Pin Manually, No Connect, and Unable To Process Pin violations.

**Figure 17. Rule Pin Name Column**



Column L is entitled Viewer Screenshot, which is a hyperlink to a Graphics Violation Viewer screen capture file in the Violations directory. There is no screen shot for Generic rules such as Duplicate Pull Up / Pull Down. Clicking on the hyperlink will open your default Jpeg viewer, most likely Internet Explorer:

**Figure 18. Screenshot Link**

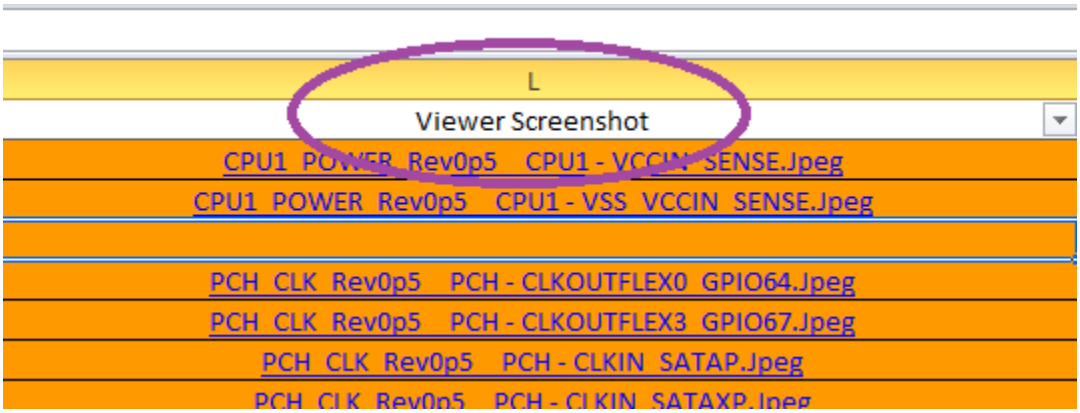
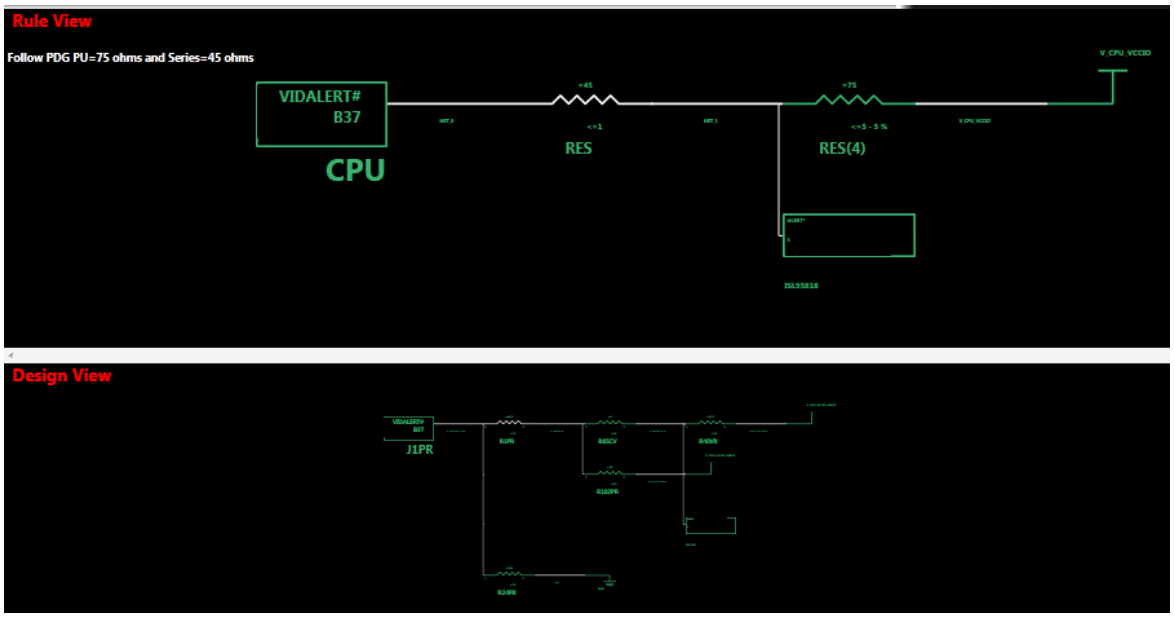



**Figure 19. Graphic Viewer Example**

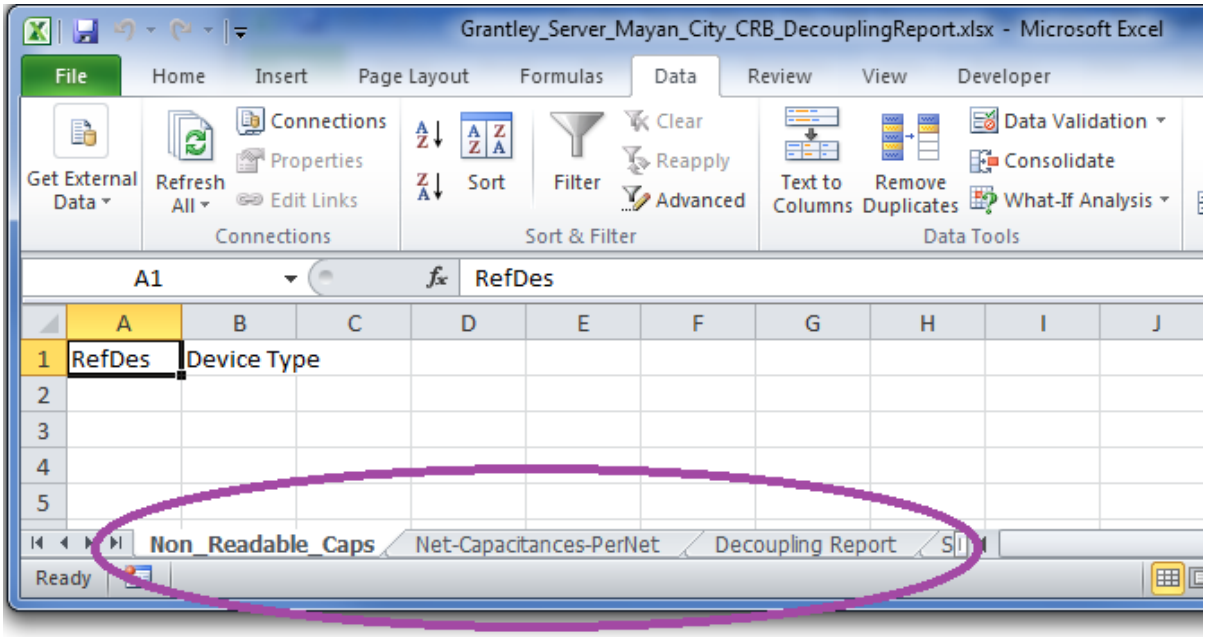


# 3 Schematic Checking Tool Decoupling Report Interpretation

The Schematic Checking Tool identifies component types, and differentiates between Voltage and Ground nets. This capability enables the production of a Decoupling Report, which is a summary of all the capacitors connected between a Voltage Net and Ground.

In the same directory where the Initial Report was found, there is a Decoupling Report. Please open it using Microsoft Excel 2010 or later:

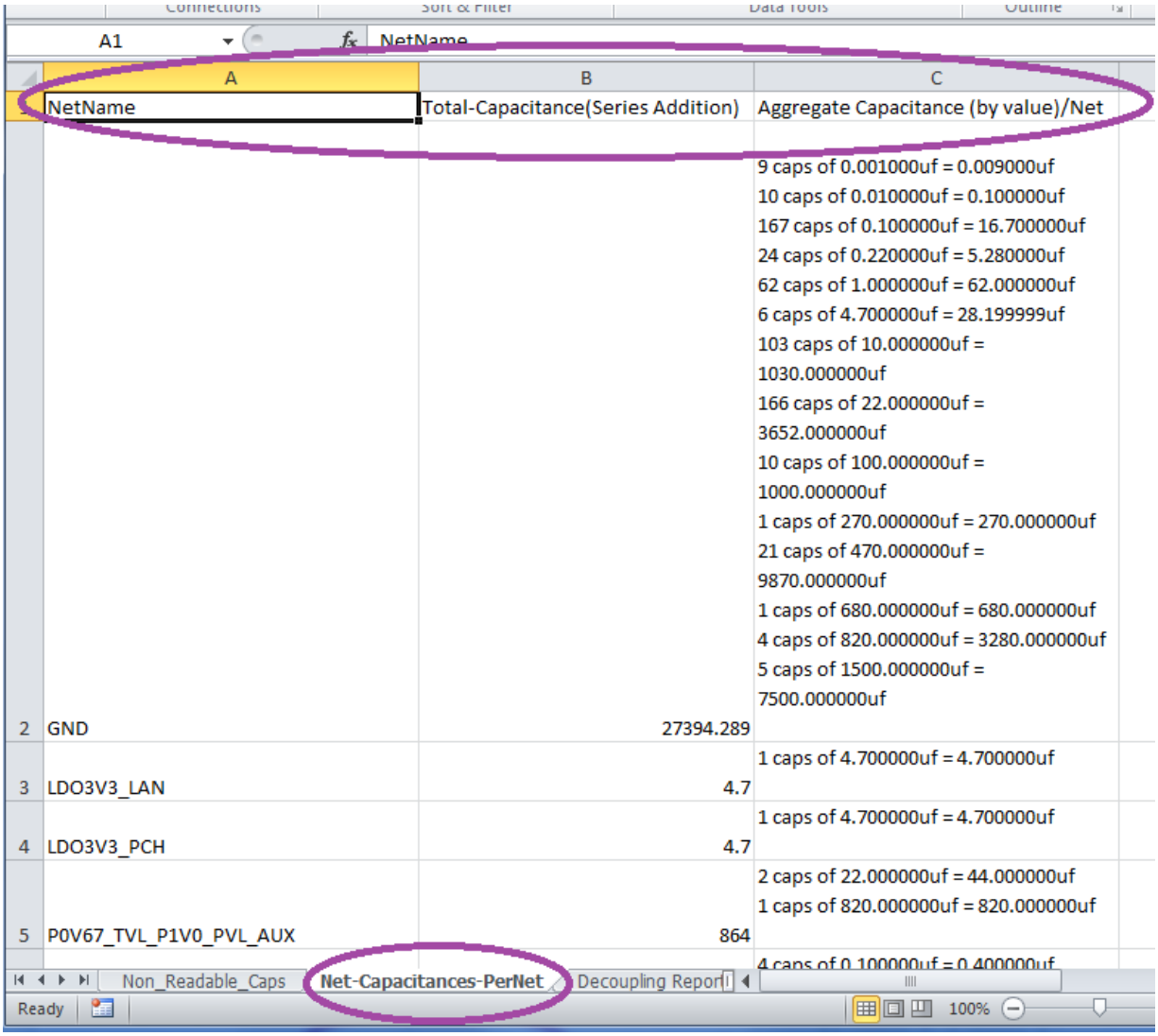
**Figure 20. Decoupling Report**




This report contains three tabs. The Non Readable Caps tab is populated with reference designators of capacitors that the Schematic Checking Tool was not able to determine the Value in Micro-Farads. This is normally and empty worksheet.

The Net Capacitance Per Net tab shows the subtotals of each capacitor Value, and the total capacitance for the net in microfarads. In designs with one single Ground net, the total shown is the total decoupling capacitance in the design (reporting by net means that Ground is a duplication of reporting elsewhere by other Voltage nets).

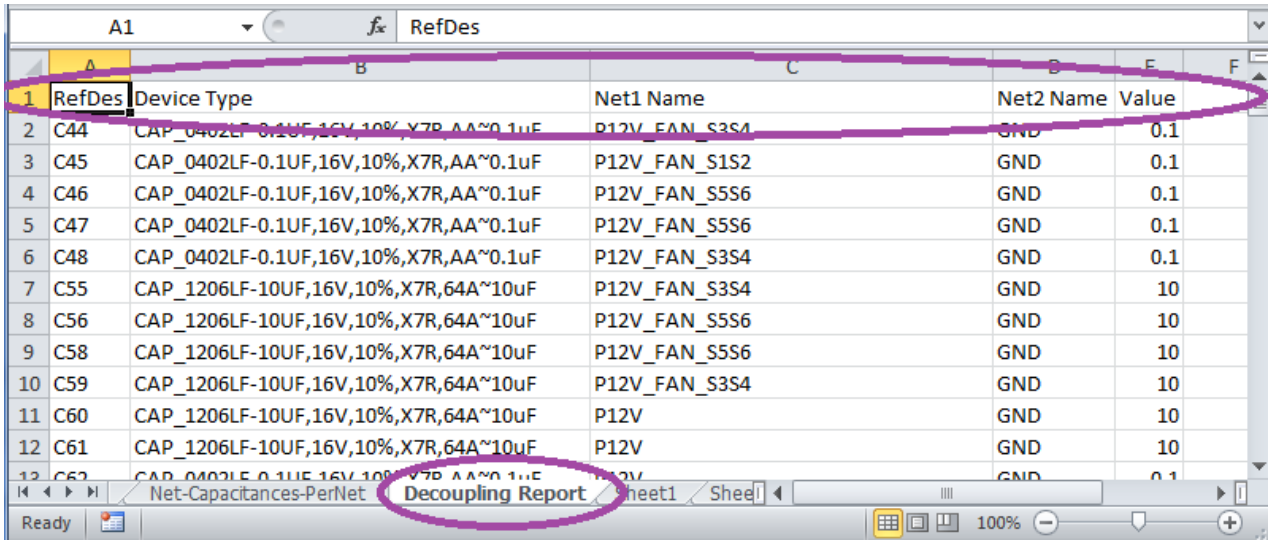
**Figure 21. Net Capacitances per Net Tab**




The advantage of this format is that it lets the reviewer see opportunities to reduce cost in their design by reducing the number of capacitor part numbers, and increasing the quantity of standardized capacitor values.

The Decoupling Report tab shows the list of Reference Designators sorted by Net Name. This enables the reviewer to see the component description, and check that the capacitor types match what is needed for each Voltage net. This also enables the reviewer to quickly identify which reference designators to find in the design, in the event that they want to make changes.

**Figure 22. Decoupling Report Tab**




| RefDes | Device Type | Net1 Name | Net2 Name | Value |
|---|---|---|---|---|
| C44 | CAP_0402LF-0.1UF,16V,10%,X7R,AA~0.1uF | P12V_FAN_S3S4 | GND | 0.1 |
| C45 | CAP_0402LF-0.1UF,16V,10%,X7R,AA~0.1uF | P12V_FAN_S1S2 | GND | 0.1 |
| C46 | CAP_0402LF-0.1UF,16V,10%,X7R,AA~0.1uF | P12V_FAN_S5S6 | GND | 0.1 |
| C47 | CAP_0402LF-0.1UF,16V,10%,X7R,AA~0.1uF | P12V_FAN_S5S6 | GND | 0.1 |
| C48 | CAP_0402LF-0.1UF,16V,10%,X7R,AA~0.1uF | P12V_FAN_S3S4 | GND | 0.1 |
| C55 | CAP_1206LF-10UF,16V,10%,X7R,64A~10uF | P12V_FAN_S3S4 | GND | 10 |
| C56 | CAP_1206LF-10UF,16V,10%,X7R,64A~10uF | P12V_FAN_S5S6 | GND | 10 |
| C58 | CAP_1206LF-10UF,16V,10%,X7R,64A~10uF | P12V_FAN_S5S6 | GND | 10 |
| C59 | CAP_1206LF-10UF,16V,10%,X7R,64A~10uF | P12V_FAN_S3S4 | GND | 10 |
| C60 | CAP_1206LF-10UF,16V,10%,X7R,64A~10uF | P12V | GND | 10 |
| C61 | CAP_1206LF-10UF,16V,10%,X7R,64A~10uF | P12V | GND | 10 |

If there are any additional questions please contact CST.Services@intel.com.