

# CST SCHEMATIC AND LAYOUT DESIGN REVIEW

**Document Requirements Quick Guide** 

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## **Schematic Design Review**

#### **Required Documents for Review**

### **1.** PDF Schematic

- a. Complete and searchable
- b. Preferable if it is non-hierarchical. If only hierarchical is available there might be a delay in completion

### 2. Board File or ISCF Extract

- a. Use to extract Netlists for automation
- b. Component placement or trace routing not required
- c. Reference designators starting with *CNxx* are not allowed. The automation always sees any component which name starts with "CN" as a 2-pin device regardless of the real pinout, causing false violations and graphic viewer captures. Please rename them.

#### **Supported File Formats**

- Cadence Allegro (.brd with 16.6, .ISCF\* with 17.2)
- Cadence OrCAD (.ISCF)
- Mentor Graphics DxDesigner (.ISCF)
- Zuken CR-5000/CR-8000 (.ISCF)
- \*ISCF = Intel Schematic Checking Format Contact <u>CST.Services@intel.com</u> for instructions

**Note:** Altium Designer, Mentor Board Station, and PADS Logic are not supported

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# **Layout Design Review**

### **Required Documents for Review**

### 1. Completely Routed Board File

- a. No DRCs, no shorts, no un-routed nets
- b. All planes completed
- c. No negative artwork if possible

### 2. Accurate Layer Stack up

- a. This can be a spreadsheet or any file format
- b. Include Dielectric Constants (Er for each layer)
- c. Include Layer Thickness
- d. If manufacturing stack up is not available, the board stack up can be used, but not recommended.

### **3.** PDF Schematic

- a. Complete and searchable
- b. Preferable if it is non-hierarchical. If only hierarchical is available there might be a delay in completion.

### **Supported File Formats**

- Cadence Allegro (.brd)
  - Support enabled for 16.6 and 17.2
- Mentor Graphics Xpedition/VX.x (.cibd, .ibd, or .cce)
- ODB++ (.tgz)
- Zuken CR-5000/CR-8000 (via ODB++)
- Altium (.hyp)



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