13th Generation Intel® Core™ Processor

Specification Update

Rev. 003
January 2023

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Contents

1. Revision History 4
2. Preface 4
3. Identification Information 6
4. Summary Tables of Changes 11
5. Errata Details 17
6. Specification Changes 37
7. Specification Clarification 38
8. Document-Only Change 38

Revision History

Revision Number	Description	Revision Date
001	Initial Release • Errata Included: RPL001-RPL034	October 2022
002	• Added Errata: RPL035, RPL036, RPL037	December 2022
003	• Added H/P, U, and HX Processor Lines	January 2023

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number
13th Generation Intel® Core™ Processors Datasheet, Volume 1 of 2	743844
13th Generation Intel® Core™ Processors Datasheet, Volume 2 of 2	743846

Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001
ACPI Specifications	www.acpi.info

Nomenclature

Errata – These are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes is incorporated in the next release of the specifications.

Specification Clarifications – This describe a specification in greater detail or further highlight a specifications impact to a complex design situation. These clarifications is incorporated in the next release of the specifications.

Documentation Changes – This include typos, errors, or omissions from the current published specifications. These changes are incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Identification Information

Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 1. Processor Lines Component Identification

Processor	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
RPL-S 8P +16E	0xB0671	Reserved	0000000b	1011b	Reserved	00b	0110b	0111b	0001b
RPL-HX 8P +16E	0xB0671	Reserved	0000000b	1011b	Reserved	00b	0110b	0111b	0001b

RPL-S 8P+ 8E	0xB 067 1	Rese rved	0000 000b	1011b	Reser ved	00b	0110 b	0111 b	000 1b
RPL-HX 8P +8E	0xB 06F 2	Rese rved	0000 000b	1011b	Reser ved	00b	0110 b	1111 b	001 0b
RPL-S 6P+ 0E	0xB 06F 2	Rese rved	0000 000b	1011b	Reser ved	00b	0110 b	1111 b	001 0b
RPL-P 6P +8E	0xB 06F 5	Rese rved	0000 000b	1011b	Reser ved	00b	0110 b	1111 b	010 1b
RPL-H 6P+ 8E	0xB 06A 2	Rese rved	0000 000b	1011b	Reser ved	00b	0110 b	1010 b	001 0b
RPL-U 2P +8E	0xB 06A 2	Rese rved	0000 000b	1011b	Reser ved	00b	0110 b	1010 b	001 0b

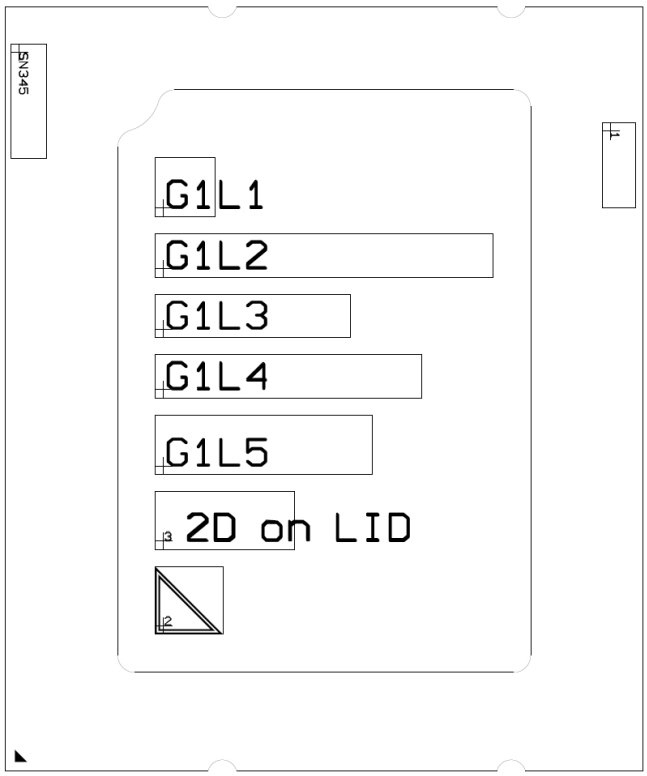
1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Celeron®, Pentium®, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model. Refer table above for the processor stepping ID number in the CPUID information.
6. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. The EDX processor signature value

after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

Component Marking Information

Figure 1. Processor Based on S-Processor Line Chip Package LGA Top-Side Markings



Pin Count: 1700 Package Size (width x height): 37.5mm x 45mm

Production (SSPEC):

- SN345
- G1L1: SPARK (Intel logo)
- G2L1: TRADEMARK BRAND
- G3L1: PROCESSOR NUMBER
- G4L1: SSPEC
- G5L1: FPO_{EX}

> **Note: Note:** "1" is used to extract the unit visual ID (2D ID).
> "2" is Pin 1 indicator on IHS.

Figure 2. Processor Based on H/P-Processor Line Chip Package LGA Top-Side Markings

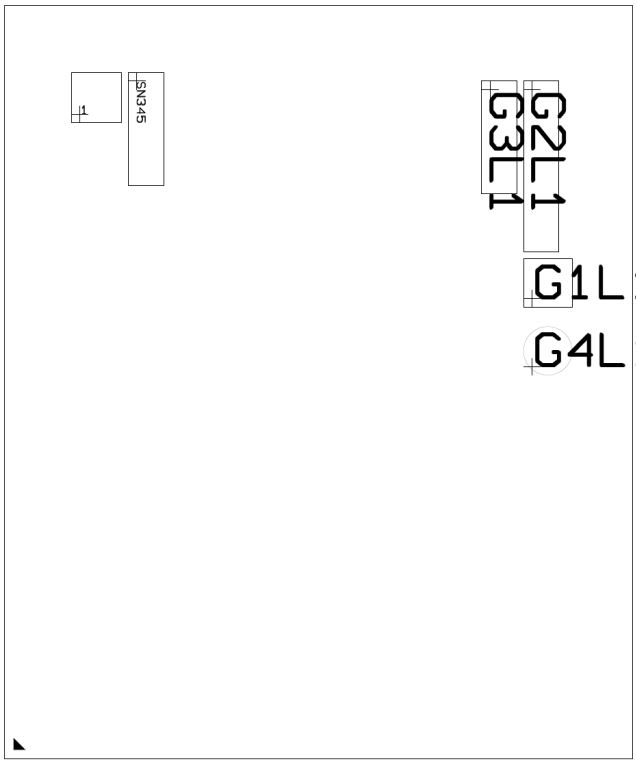
Pin Count: 1744 Package Size (width x height): 50mm x 25mm

Production (SSPEC):

- SN345
- G1L1: SPARK (Intel logo)
- G1L2: FPO
- G1L3: SSPEC
- G2L1: {ex}

Note: Note: "1" is used to extract the unit visual ID (2D ID).

Figure 3. Processor Based on HX-Processor Line Chip Package LGA Top-Side Markings



Pin Count: 1964 Package Size "(width x height)": 37.5mm x 45mm

Production (SSPEC):

- SN345
- G1L1: SPARK (Intel logo)
- G2L1: FPO
- G3L1: SSPEC
- G4L1: {eX}

> **Note: Note:** "1" is used to extract the unit visual ID (2D ID).

Figure 4. Processor Based on U-Processor Line Chip Package LGA Top-Side Markings

Pin Count: 1744 Package Size (width x height): 50mm x 25mm

Production (SSPEC):

- SN345
- G1L1: SPARK (Intel logo)
- G2L1: FPO
- G3L1: SSPEC
- G4L1: {eX}

Note: Note: "1" is used to extract the unit visual ID (2D ID).

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed processor stepping. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank Box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status	Description
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

Errata Summary Table

Erratum ID	Processor Line / Stepping							Title
	S			P/H	HX		U	
	8+16	8+8	6+0	6+8	8+16	8+8	2+8	
RPL001	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets
RPL002	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	x87 FDP Value May be Saved Incorrectly
RPL003	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP

RPL004	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® PT Trace May Drop Second Byte of CYC Packet
RPL005	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	BMI1, BMI2, LZCNT, ADXC, and ADOX Instructions May Not Generate an #UD
RPL006	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Exit Qualification For EPT Violations on Instruction Fetches May Incorrectly Indicate That The Guest-physical Address Was Writeable
RPL007	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Generate Spurious Page Faults On Shadow Stack Pages
RPL008	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Hang if Warm Reset Triggers During BIOS Initialization
RPL009	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	System May Hang When Bus-Lock Detection Is Enabled And EPT Resides in Uncacheable Memory
RPL010	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Generate Malformed TLP
RPL011	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No #GP Will be Signaled When Setting MSR_MISC_PWR_MGMT.ENABLE_SDC if MSR_MISC_PWR_MGMT.LOCK is Set

RPL012	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	PCIe Link May Fail to Train Upon Exit From L1.2
RPL013	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Incorrectly Formed PCIe Packets May Generate Correctable Errors
RPL014	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
RPL015	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Incorrect #CP Error Code on UIRET
RPL016	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	CPUID Reports Incorrect Number of Ways For The Load DTLB
RPL017	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel PT Trace May Contain Incorrect Data When Configured With Single Range Output Larger Than 4KB
RPL018	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	IA32_PERF_CAPABILITIES.PERF_METRICS_AVAILABLE is Not Set
RPL019	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	OFFCORE_REQUESTS_OUTSTANDING Performance Monitoring Events May be Inaccurate

RPL020	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	On Instructions Longer Than 15 Bytes, #GP Exception is Prioritized And Delivered Over #CP Exception
RPL021	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Mismatch on DR6 Value When Breakpoint Match is on Bitmap Address
RPL022	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	RTM Abort Status May be Incorrect For INT1/INT3 Instructions
RPL023	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Incorrect MCACOD For L2 Prefetch MCE
RPL024	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Call Instruction Wrapping Around The 32-bit Address Boundary May Return to Incorrect Address
RPL025	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	VM Entry That Clears TraceEn May Generate a FUP
RPL026	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	#UD May be Delivered Instead of Other Exceptions
RPL027	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	#GP May be Serviced Before an Instruction Breakpoint
RPL028	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Unexpected #PF Exception Might Be Serviced Before a #GP Exception

RPL029	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	WRMSR to Reserved Bits of IA32_L3_QOS_Mask_15 Will Not Signal a #GP
RPL030	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	VMX-Preemption Timer May Not Work if Configured With a Value of 1
RPL031	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing
RPL032	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
RPL033	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Unable to Transmit Modified Compliance Test Pattern at 2.5 GT/S or 5.0 GT/s Link Speeds
RPL034	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
RPL035	N/A	No Fix	N/A	N/A	N/A	N/A	N/A	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
RPL036	N/A	N/A	N/A	No Fix	No Fix	No Fix	No Fix	GPU Hang When Async Compute is Enabled

RPL037	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Type-C Host Controller Does Not Support Certain Qword Accesses

Specification Changes

No.	Specification Changes
	None for this revision of this specification update.

Specification Clarifications

No.	Specification Clarifications
	None for this revision of this specification update.

Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

Errata Details

RPL001	Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets

Problem	Some Intel Processor Trace packets should be issued only between TIP.PGE (Target IP Packet.Packet Generation Enable) and TIP.PGD (Target IP Packet.Packet Generation Disable) packets. Due to this erratum, when a TIP.PGE packet is generated it may be preceded by a PSB+ (Packet Stream Boundary) that incorrectly includes FUP (Flow Update Packet) and MODE.Exec packets.
Implication	Due to this erratum, FUP and MODE.Exec may be generated unexpectedly.
Workaround	Decoders should ignore FUP and MODE.Exec packets that are not between TIP.PGE and TIP.PGD packets.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL002	**x87 FDP Value May be Saved Incorrectly**
Problem	Execution of the FSAVE, FNSAVE, FSTENV, or FNSTENV instructions in real-address mode or virtual-8086 mode may save an incorrect value for the x87 FDP (FPU data pointer). This erratum does not apply if the last non-control x87 instruction had an unmasked exception.
Implication	Software operating in real-address mode or virtual-8086 mode that depends on the FDP value for non-control x87 instructions without unmasked exceptions may not operate properly. Intel has not observed this erratum in any commercially available software.
Workaround	None identified. Software should use the FDP value saved by the listed instructions only when the most recent non-control x87 instruction incurred an unmasked exception.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL003	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
Problem	If a MOV SS or POP SS instruction generated a debug exception, and is not followed by an explicit write to the stack pointer (SP), the processor may fail to deliver the debug exception or, if it does, the DR6 register contents may not correctly reflect the causes of the debug exception.
Implication	Debugging software may fail to operate properly if a debug exception is lost or does not report complete information. Intel has not observed this erratum with any commercially available software.
Workaround	Software should explicitly write to the stack pointer immediately after executing MOV SS or POP SS.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL004	Intel® PT Trace May Drop Second Byte of CYC Packet
Problem	Due to a rare microarchitectural condition, the second byte of a 2-byte CYC (Cycle Count) packet may be dropped without an OVF (Overflow) packet.
Implication	A trace decoder may signal a decode error due to the lost trace byte.

Workaround	None identified. A mitigation is available for this erratum. If a decoder encounters a multi-byte CYC packet where the second byte has bit 0 (Ext) set to 1, it should assume that 4095 cycles have passed since the prior CYC packet, and it should ignore the first byte of the CYC and treat the second byte as the start of a new packet.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL005	**BMI1, BMI2, LZCNT, ADXC, and ADOX Instructions May Not Generate an #UD**
Problem	BMI1, BMI2, LZCNT, ADXC, and ADOX instructions will not generate an #UD fault, even though the respective CPUID feature flags do not enumerate them as supported instructions.
Implication	Software that relies on BMI1, BMI2, LZCNT, ADXC, and ADOX instructions to generate an #UD fault, may not work correctly.
Workaround	None identified. Software should check CPUID reported instructions availability and not rely on the #UD fault behavior.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL006	**Exit Qualification For EPT Violations on Instruction Fetches May Incorrectly Indicate That The Guest-physical Address Was Writeable**
Problem	On EPT violations, bit 4 of the Exit Qualification indicates whether the guest-physical address was writeable. When EPT is configured as supervisory shadow-stack (both bit 60 in EPT paging-structure leaf entry and bit 0 in EPT paging-structure entries are set), non-executable (bit 2 in EPT paging-structure entries is cleared), and non-writeable (bit 1 in EPT paging-

	structure entries is cleared) a VMExit due to a guest instruction fetch to a supervisory page will incorrectly set bit 4 of the Exit Qualification. Bits 3, 5, and 6 of the Exit Qualification are not impacted by this erratum.
Implication	Due to this erratum, bit 4 of the Exit Qualification may be incorrectly set. Intel has not observed this erratum on any commercially available software.
Workaround	EPT handlers processing an EPT violation due to an instruction fetch access on a present page should ignore the value of bit 4 of the Exit Qualification.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL007	**Processor May Generate Spurious Page Faults On Shadow Stack Pages**
Problem	When operating in a virtualized environment, if shadow stack pages are mapped over an APIC page, the processor will generate spurious page faults on that shadow stack page whenever its linear to physical address translation is cached in the Translation Look-aside Buffer.
Implication	When this erratum occurs, the processor will generate a spurious page fault. Intel is not aware of any software that maps shadow stack pages over an APIC page.
Workaround	Software should avoid mapping shadow stack pages over the APIC page.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL008	Processor May Hang if Warm Reset Triggers During BIOS Initialization
Problem	Under complex micro-architectural conditions, when the processor receives a warm reset during BIOS initialization, the processor may hang with a machine check error reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0400H, and MSCOD (bits [31:16]) value of 0080H.
Implication	Due to this erratum, the processor may hang. Intel has only observed this erratum in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL009	System May Hang When Bus-Lock Detection Is Enabled And EPT Resides in Uncacheable Memory
Problem	On processors that support bus-lock detection (CPUID.(EAX=7, ECX=0).ECX[24]) and have it enabled (bit 2 in the IA32_ DEBUGCTL MSR (1D9h)), and employ an Extended Page Table (EPT) that is mapped to an uncacheable area (UC), and the EPT_AD is enabled (bit 6 of the EPT Pointer is set), if the VMM performs an EPT modification on a predefined valid page while a virtual machine is running, the processor may hang.
Implication	Due to this erratum, the system may hang when bus-lock detection is enabled. Intel has not observed this erratum in any commercially available software.
Workaround	VMM should not map EPT tables to Uncacheable memory while using EPT_AD.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL010	Processor May Generate Malformed TLP
Problem	If the processor root port receives an FetchAdd, Swap, or CAS TLP (an atomic operation) that is erroneous, it should generate a UR completion to the downstream requestor. If the TLP has an operand size greater than 4 bytes, the generated UR completion will report an operand size of 4 bytes, which will be interpreted as a malformed transaction.
Implication	When this erratum occurs, the processor may respond with a malformed transaction.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL011	No #GP Will be Signaled When Setting MSR_MISC_PWR_MGMT.ENABLE_SDC if MSR_MISC_PWR_MGMT.LOCK is Set
Problem	If the MSR_MISC_PWR_MGMT.LOCK (MSR 1AAh, bit13) is set, a General Protection Exception (#GP) will not be signaled when MSR_MISC_PWR_MGMT.ENABLE_SDC (MSR 1AAh, bit 10) is cleared while IA32_XSS.HDC (MSR DA0h, bit 13) is set and if IA32_PKG_HDC_CTL.HDC_PKG_Enable (MSR DB0h, bit 0) was set at least once before.
Implication	Due to this erratum, MSR_MISC_PWR_MGMT.ENABLE_SDC will be cleared even though a #GP was not signaled.
Workaround	None identified. Software should not attempt to clear MSR_MISC_PWR_MGMT.ENABLE_SDC if the above #GP conditions are met.

Status	For the steppings affected, refer to the Summary Table of Changes.

RPL012	PCIe Link May Fail to Train Upon Exit From L1.2
Problem	When the PCIe Link exits the L1.2 low-power link state, the link may fail to correctly train to L0.
Implication	Due to this erratum, a PCIe link may incur unexpected link recovery events or it may enter a Link_Down state.
Workaround	It may be possible for a BIOS code change to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL013	Incorrectly Formed PCIe Packets May Generate Correctable Errors
Problem	Under complex microarchitectural conditions, the PCIe controller may transmit an incorrectly formed Transaction Layer Packet (TLP), which will fail CRC checks.
Implication	When this erratum occurs, the PCIe end point may record correctable errors resulting in either a NAK or link recovery. Intel has not observed any functional impact due to this erratum.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL014	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
Problem	Under complex micro-architectural conditions, single step on branches (IA32_DEBUGCTLMSR (Offset 1D9h, bit [1]) and also TF flag in EFLAGS register is set) in guest might be missed when VMM enables notification on VM Exit (IA32_VMX_ PROCBASED_CTLS2 MSR, Offset 48Bh, bit [31]) while the dirty access bit is not set for the code page (bit [6] in paging-structure entry).
Implication	When single step is enabled under the above condition, some single step branches will be missed. Intel has only observed this erratum in a synthetic test environment.
Workaround	When enabling single step on branches for debugging, software should first set the dirty bit of the code page.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL015	Incorrect #CP Error Code on UIRET
Problem	If a #CP exception is triggered during a UIRET instruction execution, the error code on the stack will report NEAR-RET instruction (code 1) instead of FAR-RET instruction (code 2).
Implication	Due to this erratum, an incorrect #CP error code is logged when #CP is triggered during UIRET instruction.
Workaround	None identified.

Status	For the steppings affected, refer to the Summary Table of Changes.

RPL016	**CPUID Reports Incorrect Number of Ways For The Load DTLB**
Problem	CPUID leaf 18H sub-leaf 04H EBX [31:16] reports 4 ways instead of 6 ways for the Load DTLB.
Implication	Due to this erratum, software that relies upon the number of ways in the load DTLB may operate sub optimally.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL017	**Intel PT Trace May Contain Incorrect Data When Configured With Single Range Output Larger Than 4KB**
Problem	Under complex micro-architectural conditions, when using Intel(r) Processor Trace (PT) with single range output larger than 4KB, disabling PT and then enabling PT using the TraceEn bit in IA32_RTIT_CTL MSR (MSR 570h, bit 0) may cause incorrect output values to be recorded.
Implication	Due to this erratum, a PT trace may contain incorrect values.
Workaround	None identified. Software should avoid using PT with single range output larger than 4KB.

Status	For the steppings affected, refer to the Summary Table of Changes.

RPL018	**IA32_PERF_CAPABILITIES.PERF_METRICS_AVAILABLE is Not Set**
Problem	PERF_METRICS_AVAILABLE indication inside IA32_PERF_ CAPABILITIES MSR (bit 15 in MSR 345h) reports whether MSR_PERF_METRICS is available. This indication will not be set unless BIOS disables E-cores in the system.
Implication	When this erratum occurs, the PERF_METRICS are available even though IA32_PERF_CAPABILITIES.PERF_METRICS_ AVAILABLE reports otherwise.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL019	**OFFCORE_REQUESTS_OUTSTANDING Performance Monitoring Events May be Inaccurate**
Problem	The OFFCORE_REQUESTS_OUTSTANDING.*DATA_RD performance monitoring events (Event 20h; UMask 08h) counts the number of off-core outstanding data read transactions each cycle. Due to this erratum, an inaccurate count may be observed when Intel® HyperThreading Technology is enabled and hardware prefetchers are enabled.
Implication	OFFCORE_REQUESTS_OUTSTANDING Performance Monitoring Events may be Inaccurate.

Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL020	**On Instructions Longer Than 15 Bytes, #GP Exception is Prioritized And Delivered Over #CP Exception**
Problem	A #GP (global protection exception) that results from an instruction being longer than 15 bytes is prioritized and served before a #CP (Controlflow Protection exception) that was created due to a missing ENDBRx instruction at the target of an indirect branch.
Implication	Due to this erratum, during an indirect jump with ENDBRANCH tracking, if the processor lands on an illegal instruction with length longer than 15 bytes or that decodes to a CS limit, the processor will prioritize and deliver a #GP exception over the #CP exception.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL021	**Mismatch on DR6 Value When Breakpoint Match is on Bitmap Address**
Problem	Under complex microarchitectural conditions, on systems with Control-flow Enforcement Technology (CET) enabled, hitting a predefined data breakpoint may not be reported in B0-B3 (bits 3:0) in the DR6 register if that breakpoint was set on the legacy code page bitmap.

Implication	Due to this erratum, software may not know which breakpoint triggered when setting breakpoints on the legacy code page bitmap.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL022	**RTM Abort Status May be Incorrect For INT1/INT3 Instructions**
Problem	When Intel® Transactional Synchronization Extensions (TSX) is enabled, and there is an RTM (Restricted Transactional Memory))abort due to an INT1 or INT3 instruction, bit 5 of the RTM abort status (nested transaction execution) will not be set even if the RTM was nested.
Implication	Due to this erratum, software that manages RTM aborts cannot determine whether an abort is nested.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL023	**Incorrect MCACOD For L2 Prefetch MCE**
Problem	Under complex micro-architectural conditions, an L2 prefetch MCE that should be reported with MCACOD 165h in IA32_MC3_ STATUS MSR (MSR 40dh, bits [15:0]) may be reported with an MCACOD of 101h.

Implication	Due to this erratum, the reported MCACOD for this MCE may be incorrect.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL024	**Call Instruction Wrapping Around The 32-bit Address Boundary May Return to Incorrect Address**
Problem	In 32-bit mode, a call instruction wrapping around the 32-bit address should save a return address near the bottom of the address space (low address) around address zero. Under complex micro-architectural conditions, a return instruction following such a call may return to the next sequential address instead (high address).
Implication	Due to this erratum, In 32-bit mode a return following a call instruction that wraps around the 32-bit address boundary may return to the next sequential IP without wrapping around the address, possibly resulting in a #PF. Intel has not observed this behavior on any commercially available software.
Workaround	Software should not place call instructions in addresses that wrap around the 32-bit address space in 32-bit mode.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL025	**VM Entry That Clears TraceEn May Generate a FUP**
Problem	If VM entry clears Intel® PT (Intel Processor Trace) IA32_RTIT_CTL.TraceEn (MSR 570H, bit 0) while PacketEn is 1 then a FUP (Flow Update Packet) will precede the TIP.PGD (Target IP Packet, Packet Generation Disable). VM entry can clear TraceEn

	if the VM-entry MSR-load area includes an entry for the IA32_ RTIT_CTL MSR.
Implication	When this erratum occurs, an unexpected FUP may be generated that creates the appearance of an asynchronous event taking place immediately before or during the VM entry.
Workaround	The Intel PT trace decoder may opt to ignore any FUP whose IP matches that of a VM entry instruction.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL026	**#UD May be Delivered Instead of Other Exceptions**
Problem	An invalid instruction opcode that runs into another exception before fetching all instruction bytes (e.g. a #GP due to the instruction being longer than 15 bytes or a CS limit violation) may signal a #UD despite not fetching all instruction bytes under some microarchitectural conditions.
Implication	Due to this erratum, a #UD exception may be serviced before other exceptions. This does not occur for valid instructions. Intel has only observed this erratum in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL027	**#GP May be Serviced Before an Instruction Breakpoint**

Problem	An instruction breakpoint should have the highest priority and needs to be serviced before any other exception. In case an instruction breakpoint is marked on an illegal instruction longer than 15 bytes that starts in bytes 0-16 of a 32B-aligned chunk, and that instruction does not complete within the same 32B-aligned chunk, a General Protection Exception (#GP) on the same instruction will be serviced before the breakpoint exception.
Implication	Due to this erratum, an illegal instruction #GP exception may be serviced before an instruction breakpoint.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL028	**Unexpected #PF Exception Might Be Serviced Before a #GP Exception**
Problem	Instructions longer than 15 bytes should assert a General Protection Exception (#GP). For instructions longer than 15 bytes, a Page Fault Exception (#PF) from the subsequent page might be issued before the #GP exception in the following cases: 1. The GP instruction starts at byte 1 – 16 of the last 32B-aligned chunk of a page (starting the count at byte 0), and it is not a target of taken jump, and it does not complete within the same 32B-aligned chunk it started in. 2. The GP instruction starts at byte 17 of the last 32B-aligned chunk of a page.
Implication	Due to this erratum, an unexpected #PF exception might be serviced before a #GP exception.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL029	WRMSR to Reserved Bits of IA32_L3_QOS_Mask_15 Will Not Signal a #GP
Problem	A General Protection Exception (#GP) will not be signaled when writing non-zero values to the upper 32 bits of IA32_L3_QOS_Mask_15 MSR (Offset C9FH) even though they are defined as reserved bits.
Implication	Due to this erratum, a #GP will not be signaled when the upper bits of IA32_L3_QOS_Mask_15 are written with a non-zero value.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL030	VMX-Preemption Timer May Not Work if Configured With a Value of 1
Problem	Under complex micro-architectural conditions, the VMX-preemption timer may not generate a VM Exit if the VMX-preemption timer value is set to 1.
Implication	Due to this erratum, if the value configured to a value of 1, a VM exit may not occur.
Workaround	None identified. Software should avoid programming the VMX-preemption timer with a value of 1.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL031	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing
Problem	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT (bit 11 in MSR 1A4h) does not prevent the three-strike counter from incrementing as documented; instead, it only prevents the signaling of the three-strike event once the counter has expired.
Implication	Due to this erratum, software may be able to see the three-strike logged in the MC3_STATUS (MSR 40Dh, MCACOD = 400h [bits 15:0]) even when MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT is set.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL032	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
Problem	A VM Exit that occurs while the processor is serving a user interrupt in non-root mode should set the "asynchronous to instruction execution" bit in the Exit Qualification field in the Virtual Machine Control Structure (bit 16). However, if a VM Exit occurs during processing a user interrupt due to an APIC access, the bit will not be set.
Implication	Due to this erratum, the "asynchronous to instruction execution" bit will not be set if an APIC Access VM Exit occurs while the processor is serving a user interrupt. Intel has not observed this erratum with any commercially available software.

Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL033	**Unable to Transmit Modified Compliance Test Pattern at 2.5 GT/S or 5.0 GT/s Link Speeds**
Problem	The processor's PCIe port (Bus 0, Device 1, Function 0/1/2 or Bus 0, Device 6, Function 0) does not transmit the Modified Compliance Test Pattern when in either 2.5 GT/S or 5.0 GT/s link speeds.
Implication	Due to this erratum, PCIe compliance testing may fail at 2.5 GT/S or 5.0 GT/s link speeds when enabling the Modified Compliance Test Pattern.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL034	**USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst**
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.

Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL035	**Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results**
Problem	The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC.Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.
Implication	In this case the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL036	**GPU Hang When Async Compute is Enabled**

Problem	GPU may hang when Async Compute is enabled
Implication	Due to this erratum, the GPU may hang when running high bandwidth GFx application such as benchmarks and/or games.
Workaround	None identified. The Async Compute feature will be disabled in a graphics driver update. See GFx Driver Revenue SV2 PR5 (101.3616 or later) and release notes.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL037	**Type-C Host Controller Does Not Support Certain Qword Accesses**
Problem	The Type-C controller does not properly support Qword accesses to its MSI-X interrupt table which may lead to unexpected behavior.
Implication	When this erratum occurs, Qword reads do not return Unsupported Request and may not return correct data and Qword writes may lead to unexpected behavior. Intel has not observed this erratum to affect any commercially available software.
Workaround	Software should not utilize Qword access for the Type-C MSI-X table.
Status	For the steppings affected, refer to the Summary Table of Changes.

Specification Changes

None.

Specification Clarification

None.

Document-Only Change

None.